## REMARKS

Claims 1-17 are pending.

Claims 1, 11 and 13 are rejected.

Claims 12 and 14 are objected to.

Claims 2-10 and 15-17 are allowed.

## EXAMINER INTERVIEW

The Applicant called the Examiner because the Examiner cited new grounds for rejecting Claims 1, 11 and 13 and made the rejection final. The Examiner called back and said it was a mistake and would send a supplemental response indicating the rejection was not final.

## I. REJECTION UNDER 35 U.S.C. § 102

The Examiner rejected Claims 1, 11, and 13 under *35 U.S.C. § 102(b)* as being anticipated by U.S. Patent No. 5,604,450 to *Borkar* (hereafter " *Borkar*").

For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

The Examiner states that *Borkar* discloses the digital transmission system of Claim 1. The invention of *Borkar* is directed to a (simultaneous) bi-directional signaling scheme where the line driver has four possible states; it is driving a logic one while receiving a logic zero or one and driving a logic zero while receiving a logic zero or a logic one. Claim 1 recites a first driver circuit receiving a first data input signal and generating a first driver output signal in response to a clock signal, wherein the first driver output is coupled to a first input of a first transmission line. The Examiner cites

Fig. 2, Fig. 3 and Fig. 5 of *Borkar* as teaching element DRVA as the first driver circuit, element COA as the first data input signal, element N1 as the first driver output signal, elements EN0-EN3 and EN0_bar-EN3_bar (Fig. 5) as the clock signal, and element Z0 as the first transmission line. The Applicant asserts that the signals EN0-EN3 and EN0_bar-EN3_bar are not clock signals, rather they are enable signals that determine how many devices are gated ON in parallel when driving either a logic 1 or a logic zero. *Borkar* states that "one way this can be accomplished is to use a chip scan chain using external scan data and control signals to set EN0, EN1, EN2, EN3 and their inverses to enable the correct number of legs of the transistors within box 61 as is well known in the art. This operation is performed one time and accounts for process variations but not voltage and temperature variations which may exist when the part is being used." Clearly *Borkar* states the signals ENX are not clock signals and that they are not used to compensate for voltage changes. Also in Fig. 3 there are three transmission lines labeled Z0; the Examiner did not specifically point out which Z0 he was referring to relative to his rejection of Claim 1.

Claim 1 also recites a receiver circuit having a first receiver input coupled to the first output of the first transmission and a second receiver input coupled to a reference voltage. The Examiner again cites Fig. 2, Fig. 3 and Fig. 5 of *Borkar* as teaching element DIFFB as the first receiver circuit, the positive input of DIFFB as the first receiver input coupled to the first output of the first transmission line, the negative input of DIFFB as the second receiver input coupled to a reference voltage REFB.

Finally, Claim 1 recites a first termination network receiving program signals and generating a first terminating voltage with a first source impedance at a first node coupled to the first output of the first transmission line, wherein the first termination voltage is modified in response to the first programming signals while maintaining a pre-determined magnitude of the first source impedance. The Examiner states the DRVB in Fig. 5 is the first terminating network and the ENX signals are the program signals. First, the Examiner has stated that the signals ENX are both clock signals and program signals. Secondly, the Applicant has shown where *Borkar* clearly states that using different

values for ENX does not compensate for voltage changes. Since the ENX signals are complement signals, either one or multiple of the PFET devices in DRVB of Fig. 5 are enabled in response to the ENX signals and turned ON in response to a logic zero at IN or one or all of the NFET devices in DRVB of Fig. 5 are enabled in response to the ENX signals and turned ON response to a logic one at IN. Therefore, in the embodiment when ENX signals are complements, the Applicant asserts that while the drive level impedance of DRVB in *Borkar* may be changed, the drive level impedance is not maintained at a pre-determined magnitude while modifying the first terminating voltage response to the programming signals as recited in Claim 1.

In the embodiment cited by the Examiner, the Examiner states that the disclosure of *Borkar* (Fig. 2, Fig. 3 and column 3, line 3 through column 6, line 21) teaches signals ENX and ENX_bar can be externally controlled or programmed by a state machine for compensating voltage and temperature variations. In this recitation, *Borkar* states the following; "an alternate approach is to use an external resistor which is an input to a state machine which provides the EN0, EN1, EN2, EN3 signals and their inverses. This approach uses just one external pin and a well behaved resistor which allows for temperature and voltage variations to be compensated for. The specifics for implementing a suitable state machine and resistor should be readily apparent to persons skilled in the art." The Applicant contends that this cited embodiment of *Borkar* is not enabled. *Borkar* gives not indication of how the single resistor is used to generate ENX and ENX_bar signals that would result in varying the voltage at the receiver first node while maintaining a pre-determined magnitude of the first source impedance as recited in Claim 1.

The Examiner has stated the one set of elements (ENX, ENX_bar) must have two completely different functionalities (clock and programming signals) for the disclosure of *Borkar* to read on clock and programming signals of Claim 1. Further, the Applicant asserts that the Examiner relies on non-enabled disclosure in *Borkar* to read on the terminating network of Claim 1. For these reasons, Applicant respectfully asserts that

the Examiner has failed to make a *prima facie* case of anticipation under *35 U.S.C. § 102(b)* over *Borkar*.

Therefore, the Applicant respectfully asserts that the rejection of Claim 1 under *35 U.S.C. § 102(b)* as being anticipated by *Borkar* is traversed by the above arguments.

Claim 11 is directed to a data processing system having a CPU IC with off-chip drivers incorporating the digital signal transmission system of Claim 1. The Applicant has shown that *Borkar* does not anticipate the invention of Claim 1, therefore *Borkar* does not anticipate the data processing system of Claim 11 incorporating the invention of Claim 1.

The Applicant, therefore, respectfully asserts that the rejection of Claim 11 under *35 U.S.C. § 102(b)* as being anticipated by *Borkar* is traversed by the above arguments and for the same reasons as Claim 1.

Claim 13 is an independent claim directed to a signal transmission system that has limitations not recited in Claim 11. The Examiner rejected Claims 13 for the same reasons as Claim 11. The Applicant asserts that the Examiner has failed to make a *prima facie* case of anticipation for failing to specifically address the invention of Claim 13. Therefore, the Application further asserts that the rejection of Claim 13 under *35 U.S.C. § 102(b)* as being anticipated by *Borkar* is traversed by the above arguments and for the same reasons as Claim 11.

## II. CLAIM OBJECTIONS

Claim 12 is dependent from Claim 11. Claim 12 is objected to as depending from rejected Claim 11. The Examiner did not specifically say that Claim 12 had allowable material. The Applicant has rewritten Claim 12 in independent form to include the limitations of Claim 11, however, Applicant has argued that Claim 11 is allowable over the cited prior art.

Claim 14 is dependent from Claim 13. Claim 12 is objected to as depending from rejected Claim 11. The Examiner did not specifically say that Claim 14 had allowable material. The Applicant has rewritten Claim 14 in independent form to include the limitations of Claim 13, however, Applicant has argued that Claim 13 is allowable over the cited prior art.

## III. CONCLUSION

The rejection of Claims 1, 11, and 13 under *35 U.S.C. § 102(b)* over *Borkar* have been traversed.

Claims 2-10 and 15-17 are allowed and the Applicant thanks the Examiner for allowing these claims.

The objections of Claims 12 and 14 have been traversed by writing these claims in independent form including the limitations of Claims 11 and 13 from which they respectively depend.

Therefore the Applicant asserts that now Claims 1, 11, 12, 13, and 14 are also in condition for allowance and requests early allowance these claims.

Applicants respectfully request that the Examiner call Applicant's attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,
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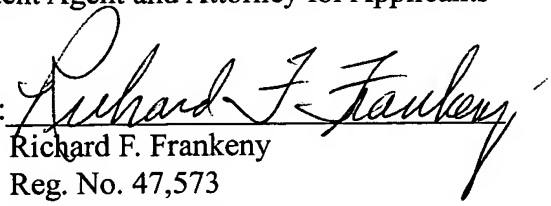
By: 
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